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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 23/532, 23/528, 21/48, 21/768

A1

(11) International Publication Number: **WO 99/67823**

(43) International Publication Date: 29 December 1999 (29.12.99)

(21) International Application Number: PCT/IB99/01129

(22) International Filing Date: 17 June 1999 (17.06.99)

(30) Priority Data:
98/07935 23 June 1998 (23.06.98) FR

(71) Applicants *(for all designated States except US)*: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL–5621 BA Eindhoven (NL). STMICROELECTRONICS S.A. [FR/FR]; 7, avenue Gallieni, F–94250 Gentilly Cedex (FR).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: LOUWERS, Stephan [NL/FR]; 850, rue Jean Monnet, F–38926 Crolles (FR). MARTY, Michel [FR/FR]; 7, avenue Gallieni, F–94250 Gentilly Cedex (FR).

(74) Agent: DUIJVESTIJN, Adrianus, J.; Prof. Holstlaan 6, NL–5656 AA Eindhoven (NL).

(81) Designated States: JP, US, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: INTEGRATED CIRCUIT HAVING A LEVEL OF METALLIZATION OF VARIABLE THICKNESS

(57) Abstract

An integrated circuit comprising at least one level of metallization, the level of metallization being provided with tracks and comprising metal portions having at least two different thicknesses. The level of metallization comprises at the same time at least one inductor and at least one track, the track being formed on a portion of small thickness, and the inductor being formed on a portion of large thickness.

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Integrated circuit having a level of metallization of variable thickness

The invention relates to an integrated circuit comprising at least one level of metallization, the level of metallization being provided with tracks and comprising metal portions of at least two different thicknesses.

A level of metallization usually comprises metal tracks of small thickness, for example 1 micron, and small width, for example 1 micron. These metal tracks are used to transfer logic data. To manufacture inductors with an inductance of several nanohenrys, a separate level of metallization may be provided which is employed only for this purpose. In order to reduce the resistance of these inductors, particularly the direct-current resistance, use is made of inductors having a large width of, for example, 20 µm, and a large thickness of, for example, 2.5 µm.

However, it is rather unsatisfactory to use a level of metallization only for inductors as a large area of this level of metallization remains unused. For this reason it would be desirable to take measures enabling said level of metallization to also comprise tracks for the transfer of logic data, said tracks having a small width. However, it is very difficult to manufacture tracks which are narrow and thick.

It is an object of the present invention to provide an integrated circuit having a level of metallization comprising both an inductor and a track for, for example, transfer of logic data.

To achieve this, the integrated circuit in accordance with the invention is characterized in that the level of metallization comprises at the same time at least one inductor and at least one track, the track being formed on a portion of small thickness, and the inductor being formed on a portion of large thickness.

The coupling between the turns of wire of the inductor is only slightly affected by the profiles of the portions having a large thickness, which include a first part at the bottom of the step having a straight edge and a second concave part.

In an embodiment of the invention, the level of metallization comprises a first metal layer and a second metal layer, which are separated by a stop layer. The second metal layer may have a larger thickness than the first metal layer.

A further object of the invention is to provide a method of manufacturing a level of metallization of an integrated circuit, the level of metallization being provided with tracks. A first metal layer is provided, whereafter a stop layer and a second metal layer are applied. A first mask of a resin is provided on the circuit. The second metal layer is subjected to photoetching down to the stop layer. A second resin mask is deposited on the circuit. The stop layer and the first metal layer are etched, in such a manner that portions comprising the first metal layer and the second metal layer and portions comprising only the first metal layer remain intact.

After photoetching the second metal layer, the first mask may be removed or preserved.

In this manner, an integrated circuit is obtained wherein the use of a level of metallization is optimized, which enables the number of levels of metallization to be reduced, resulting in a smaller thickness of the integrated circuit and in a saving in costs owing to the smaller number of process steps, or, the performance of the integrated circuit to be increased if the number of levels of metallization remains unchanged.

These and other aspects of the invention will be apparent from and elucidated, by way of non-limitative example, with reference to the embodiment(s) described hereinafter.

In the drawings:

Figs. 1a through 1f are diagrammatic, cross-sectional views of a method in accordance with the invention; and

Figs. 2a through 2f show a modification of the preceding Figures.

As shown in Fig. 1a, a first metal layer 2 is deposited, in a thickness of approximately 1 µm, on the upper dielectric layer 1 of an integrated circuit. Subsequently, a stop layer 3 having a small thickness of, for example, 300 Å is deposited on the first metal layer 2. This stop layer 3 may be made from titanium or titanium nitride. Next, a second metal layer 4, having a thickness of for example 2 µm, is deposited.

In the step shown in Fig. 1b, a first resin mask 5 is provided on the second metal layer 4. The areas protected by the mask 5 are defined by means of a photorepeater.

Fig. 1c shows that the second metal layer 4 is subjected to an etching process, i.e. an isotropic wet etching process. By means of said wet etching process the second metal

layer 4 can be removed, with the exception of the regions protected by the mask 5. However, the regions 6 of the second metal layer 4 adjoining the lateral edges 5a of the mask 5 are subject to erosion during said wet etching process. This erosion results in a concave lateral edge of the second metal layer 4. Etching stops at the stop layer 3 by virtue of the selectivity of the process with respect to a titanium nitride layer. In this manner the future portions of large thickness of the level of metallization of the integrated circuit are defined.

Fig. 1d shows that, subsequently, the mask 5 is removed.

Next, a second resin mask 8 is provided, see Fig. 1e. This mask 8 covers the regions previously covered by the first mask 5, which regions are used to form the portions of large thickness, and it covers other, previously etched, regions which serve to form portions of small thickness. Next, the integrated circuit is etched in a plasma-anisotropic process, so that the regions of the stop layer 3 and the first metal layer 2 which are not protected by the mask 8 are removed. As described hereinabove, the resin mask 8 is subsequently removed.

As shown in Fig. 1f, two types of patterns are obtained. A first type is formed by the portions of large thickness 9, which are composed of the first metal layer 2, the stop layer 3 and the second metal layer 4, and a second type is formed by portions of small thickness 10 which are composed only of the first metal layer 2 and the stop layer 3, the plasma-etching process having stopped at the dielectric layer 1. The portions of large thickness 9 may be used as inductors having a thickness above 3 μm and a width of the order of 20 μm, while the portions of small thickness 10 constitute tracks of a logic circuit, their thickness and width ranging between 1 and 1.5 μm.

It is noted that the concave edges 7 of the portions of large thickness 9 have not been modified by the plasma-etching step because they were covered with the second resin mask 8, see Fig. 1e. As a result, the portions of large thickness 9 comprise an edge having a complex profile, i.e. the concave edge 7 at the level of the second metal layer 4 and a straight edge 11 at the level of the first metal layer 2. This arrangement does not present any drawback in terms of reduction of the section of portion 9, because the surface of the region 6 where the metal of the layer 4 has been removed is very small with respect to the whole of the portion of large thickness 9.

As a matter of fact, it is assumed that the width of the region 6 will be smaller than or equal to the thickness of the second metal layer 4 wherein it has been formed. The portion of large thickness 9 will have maximally lost, at its top part, a part of its width which corresponds to approximately twice the thickness of the second metal layer 4. The resistance value is not significantly increased thereby. An advantage of a profile having two slopes is that

it has an obtuse angle at the top of the step. By virtue of this characteristic, the concentration of stresses in the upper passivating layer of the circuit is limited. In short, this method enables inductors having a very large thickness, of for example, 4 µm to be obtained, which cannot be manufactured in a single metal layer since etching of such a layer would require the deposition of a resin layer in a thickness equal to that of the inductor, which could not be insulated in a suitable manner.

In practice, this method can be used in combination with a first metal layer having a thickness ranging between 0.6 and 1 µm and a second metal layer having a thickness ranging between 1 and 4 µm.

The deposition of the three layers, i.e. first metal layer, stop layer and second metal layer, can be carried out one after the other, thereby achieving substantial savings in the production process.

The embodiment shown in Figs. 2a through 2f is similar to the preceding embodiment, with the exception that the first resin mask 5, which is shown for example in Fig. 2c and which protects the second metal layer 4, is not removed but preserved for the following step shown in Fig. 2d wherein the second resin mask 8 is deposited and, subsequently, developed in a second photolithographic step, which results in the circuit shown in Fig. 2e.

This modification of the method enables the precision of the etching process to be increased. As a matter of fact, the portion of large thickness 9 is defined only by the first mask 5, while the portions of small thickness 10 are defined only by the second mask 8. In this manner, any mistake in repositioning the photorepeater during the development of the second mask is avoided, which mistake could cause a relative displacement of the first metal layer 2 and the second metal layer 4 forming the portions of large thickness 9.

By virtue of the invention, an integrated circuit is obtained having metal portions of different thicknesses for the same level of metallization, which enables a better use of said level of metallization.

CLAIMS:

1. An integrated circuit comprising at least one level of metallization, the level of metallization being provided with tracks and comprising metal portions (9, 10) of at least two different thicknesses, characterized in that the level of metallization comprises at the same time at least one inductor and at least one track, the track being formed on a portion of small thickness (10), and the inductor being formed on a portion of large thickness (9).

2. A circuit as claimed in claim 1, characterized in that the portion of large thickness (9) comprises a first part having a straight edge (11) and a second part having a concave edge (7).

3. A circuit as claimed in any one of the preceding claims, characterized in that the level of metallization comprises a first metal layer and a second metal layer, which are separated by a stop layer (3).

4. A circuit as claimed in claim 3, characterized in that the thickness of the second metal layer (4) is larger than the thickness of the first metal layer (2).

5. A method of manufacturing a level of metallization of an integrated circuit, the level of metallization being provided with tracks, according to which method, a first metal layer is deposited, a stop layer is deposited, a second metal layer is deposited, a first resin mask is deposited, the second metal layer is photoetched down to the stop layer, a second resin mask is deposited, and the stop layer and the first metal layer are photoetched in such a manner that portions comprising the first metal layer and the second metal layer and portions comprising only the first metal layer remain intact.

6. A method as claimed in claim 5, wherein the first mask is removed after the second metal layer has been subjected to a photoetching process.

7. A method as claimed in claim 5, wherein the first mask is preserved after the second metal layer has been subjected to a photoetching process.

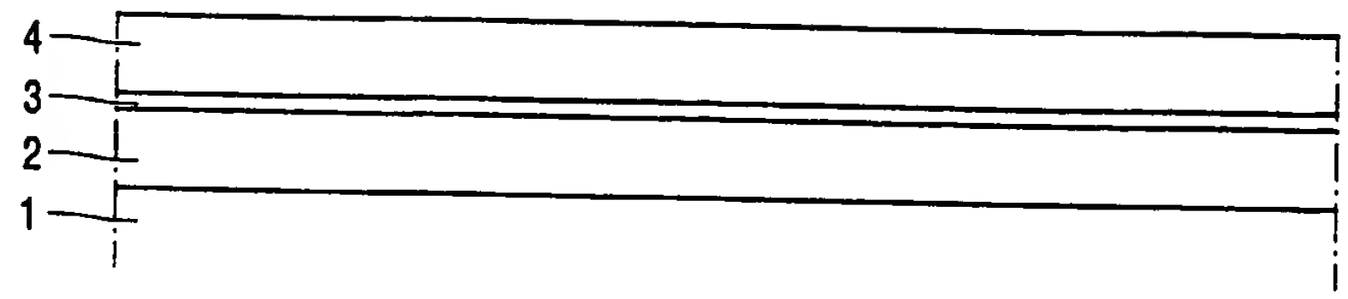

FIG. 1a

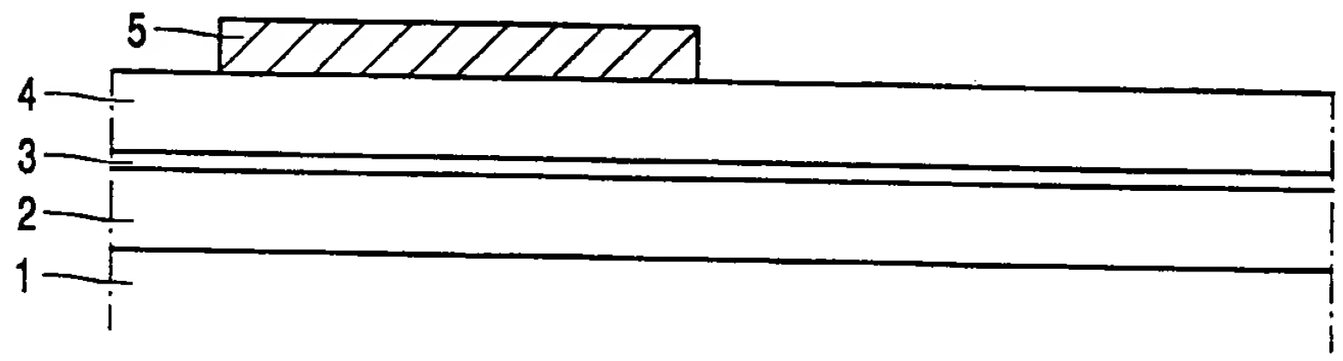

FIG. 1b

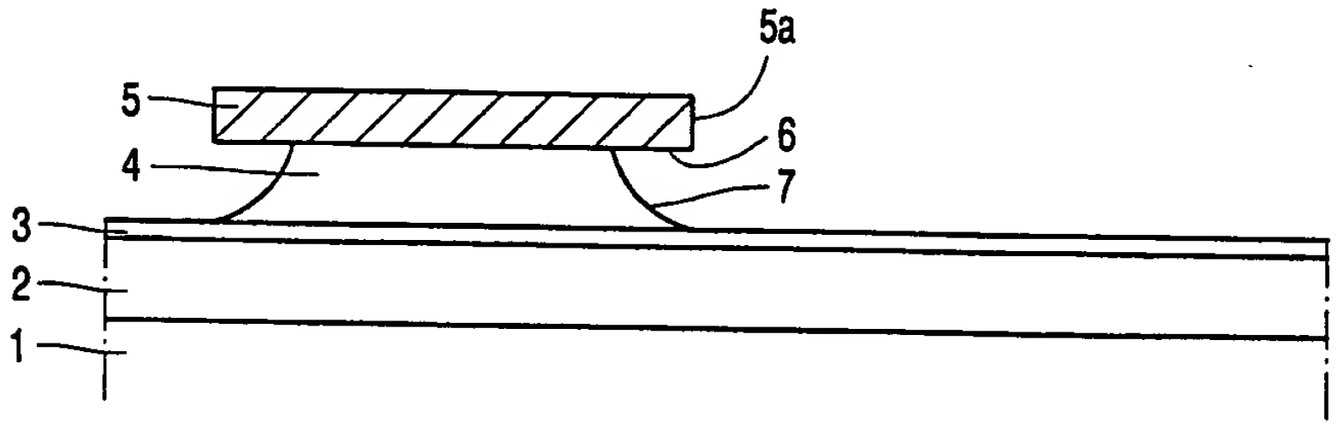

FIG. 1c

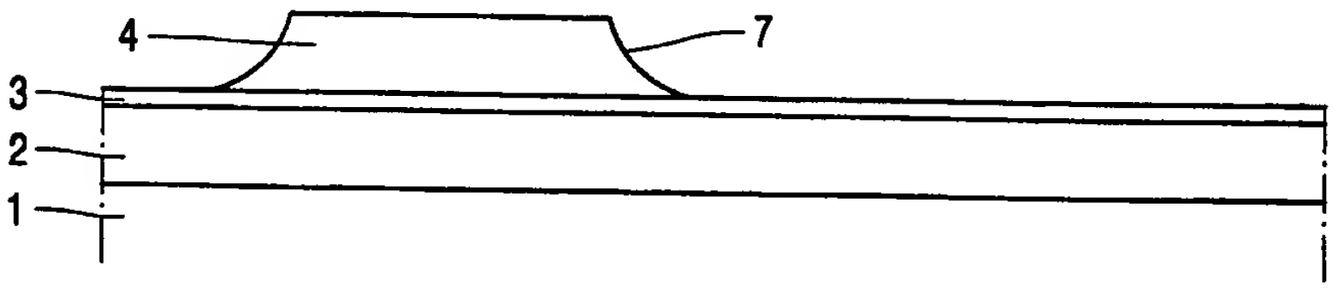

FIG. 1d

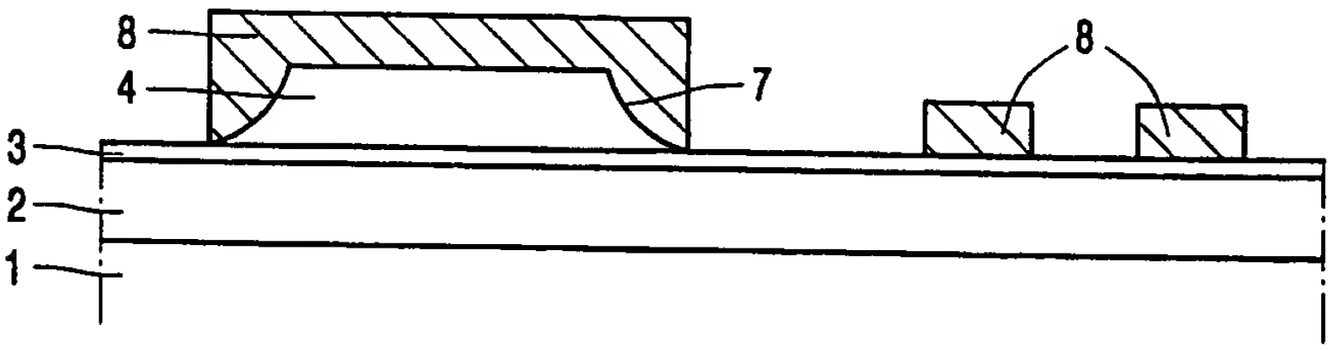

FIG. 1e

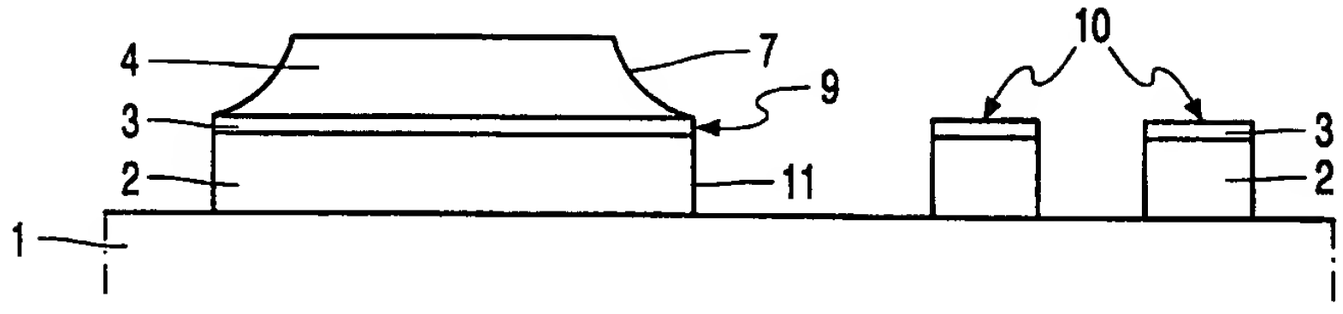

FIG. 1f

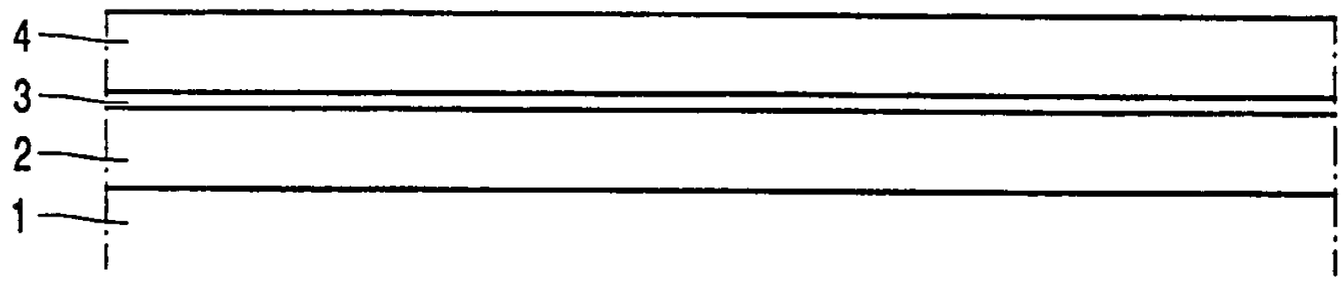

FIG. 2a

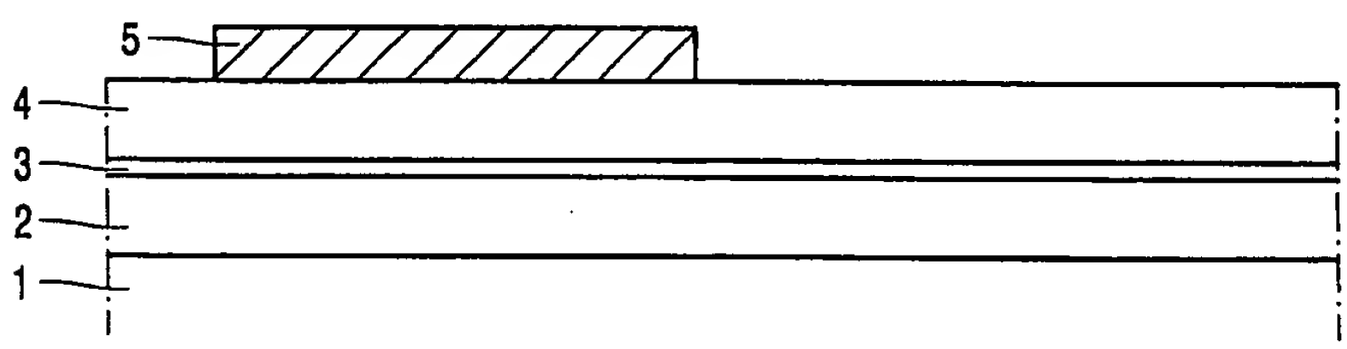

FIG. 2b

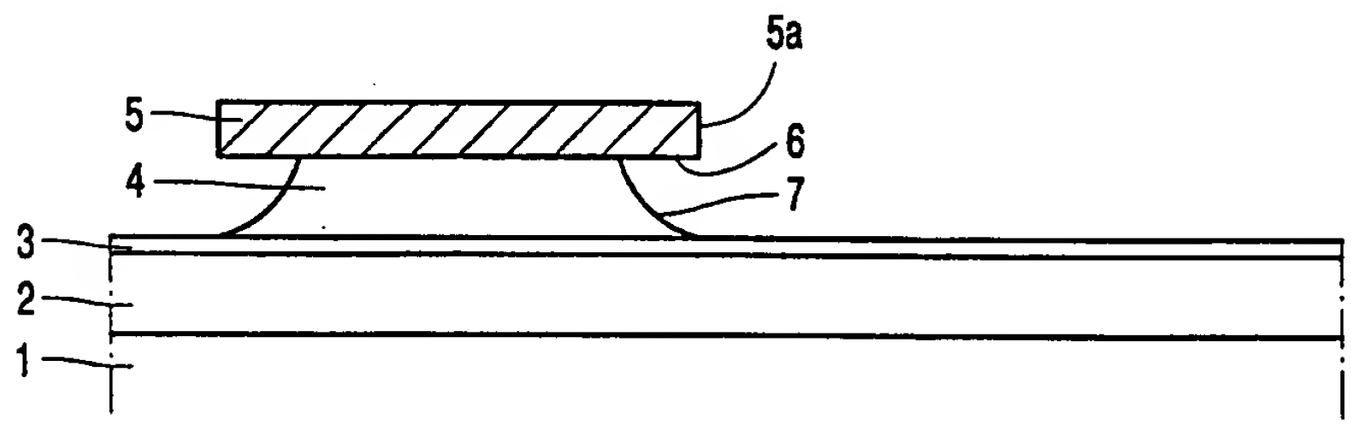

FIG. 2c

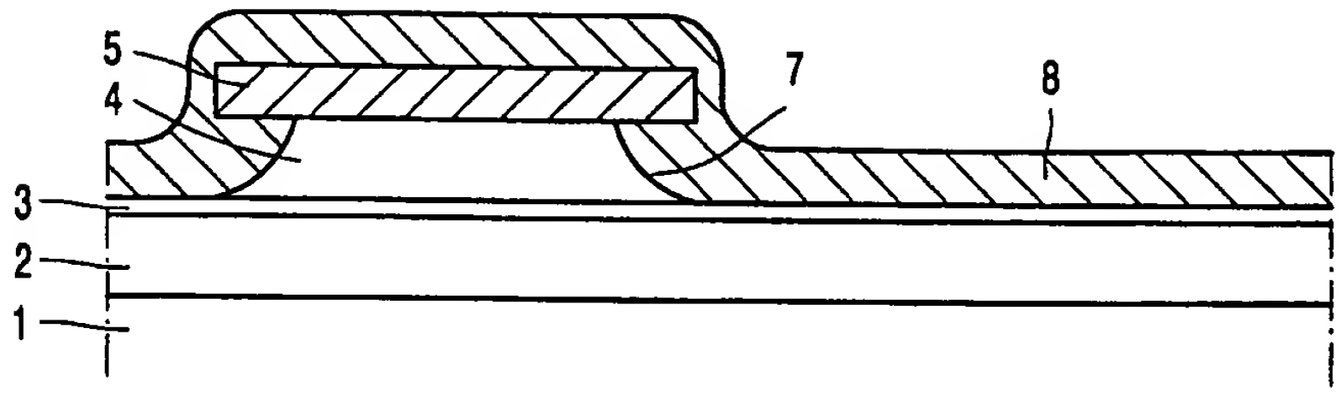

FIG. 2d

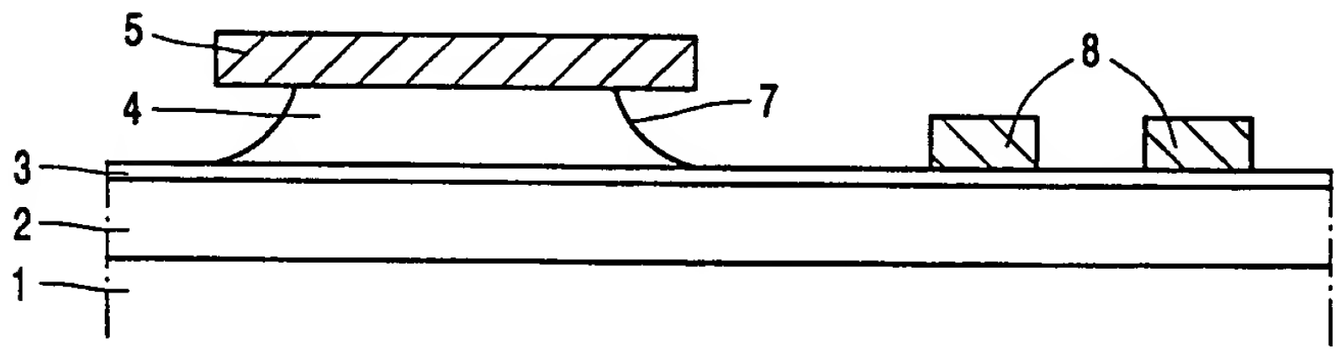

FIG. 2e

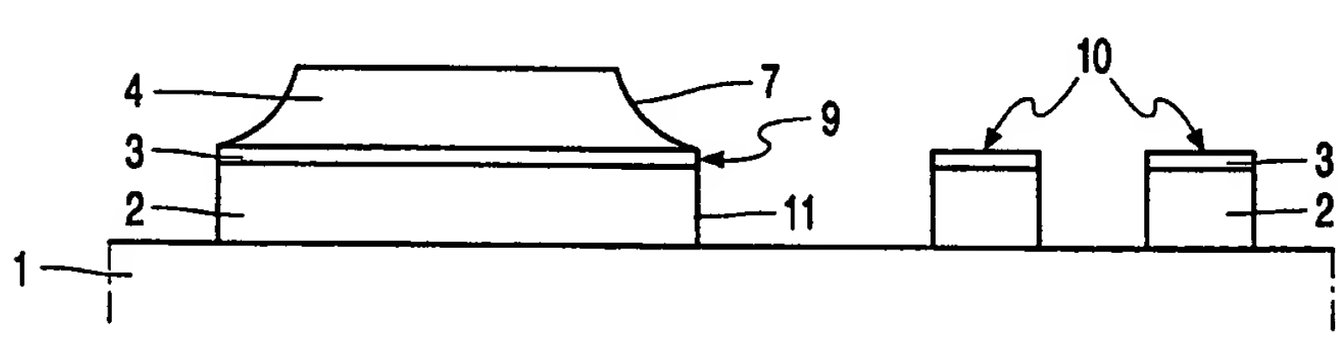

FIG. 2f

INTERNATIONAL SEARCH REPORT

	It .ational Application No PCT/IB 99/01129

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L23/532 H01L23/528 H01L21/48 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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X	EP 0 706 211 A (ITT IND GMBH DEUTSCHE) 10 April 1996 (1996-04-10) figure 5 ---	1
X	US 5 652 157 A (HIRANO MAKOTO ET AL) 29 July 1997 (1997-07-29) column 1, line 18 - line 55 column 22, line 20 - column 23, line 4 column 23, line 49 - column 24, line 43 figures 35-39,43 ---	1,2

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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